

What is claimed is:

1. An electrode line structure of a semiconductor device comprising:
a semiconductor substrate; and
electrode lines formed on the semiconductor substrate, the electrode lines having
an inclined end in the long axis direction;

wherein the electrode lines each include a first line unit, which substantially
functions as an electrode line, a second line unit, which includes the inclined end in the
long axis direction and which is separated from the first line unit by a predetermined
distance, and an insulating plug, which is interposed between the first line unit and the
second line unit and electrically insulates the first line unit from the second line unit.

2. The electrode line structure of claim 1, wherein the length of the electrode
lines is greater than an ordinary length of conventional electrode lines by a
predetermined length.

3. The electrode line structure of claim 2, wherein the insulating plug is
formed at a predetermined position of each of the electrode lines such that the first line
unit has the ordinary length.

4. The electrode line structure of claim 1, wherein the length of the second
line unit is greater than a width of the electrode lines and less than the ordinary length.

5. The electrode line structure of claim 1, wherein the first line unit and the
second line unit each comprise a conductive layer and a hard mask layer, respectively.

6. The electrode line structure of claim 5, wherein the conductive layer
comprises a material containing tungsten.

7. The electrode line structure of claim 5, wherein the hard mask layer
comprises a silicon nitride layer or a silicon oxynitride layer.

8. The electrode line structure of claim 1, wherein a spacer is formed on the inclined end in the long axis direction of the second line unit.

9. The electrode line structure of claim 8, wherein the insulating plug is formed of a material of which the spacer is formed.

10. The electrode line structure of claim 1, wherein the electrode lines comprise one of word lines and bit lines.

11. A method of forming an electrode line structure of a semiconductor device, comprising:

depositing a conductive layer on a semiconductor substrate;

depositing a hard mask layer on the conductive layer;

patterning the hard mask layer and the conductive layer to form electrode lines;

forming a hole of a line shape in a predetermined portion of each of the electrode lines to cut the electrode lines, thereby defining a separated first line unit and second line unit;

depositing an insulating layer in the hole and on the electrode lines; and

etching the insulating layer using an anisotropic etching method to form a spacer at an edge of the electrode lines.

12. The method of claim 11, wherein the conductive layer comprises a material containing tungsten.

13. The method of claim 11, wherein the hard mask layer comprises a silicon nitride layer or a silicon oxynitride layer.

14. The method of claim 11, wherein the length of the electrode lines is greater than an ordinary length of conventional electrode lines by a predetermined length.

15. The method of claim 14, wherein the hole is formed at a predetermined position of each of the electrode lines such that the first line unit has the ordinary length.

5 16. The method of claim 15, wherein the width of the hole in a direction perpendicular to a long axis of each electrode line is less than two times the thickness of the insulating layer.

17. The method of claim 14, wherein a length of the second line unit is greater than a width of the electrode lines and less than the ordinary length.

10 18. The method of claim 11, wherein the electrode lines comprise one of word lines and bit lines.